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Can You Continue to Profit by Moore's Law?

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Blindly following Moore's Law to smaller geometries is leading the fabless integrated circuit (IC) companies (FICC) to a profitless cliff. Rising design and process costs are leading the FICC down the road to perdition. It's clear that design and process costs are escalating to a point where the intended application markets can't support the build cost. The result is that the integrated circuit (IC) vendor can't amortize those costs to achieve profitability.

Much like the PC industry, the FICC has enjoyed the benefits of standardization by leveraging standard tooling for ever-smaller design geometries and the use of ubiquitous CMOS process technology. For the prudent semiconductor businessman this led to a profitable business model, delivering a high return on investment (ROI) to investors. However, the end is near. In the worst possible scenario, the fabless semiconductor industry may soon look more like the disk-drive business than the wild and wooly IC industry of 1995. The profile of an industry wracked by shortening product cycles, customer demands for low fixed end-price points and declining profitability. The disk-drive industry models a saw tooth volume and pricing model (order stocking model) versus the traditional learning curve (Moore's Law) seen in the semiconductor industry.

The reason for this nightmare is that we have reached the time where the Moore's Law and the primary law of finance (profitability) approach their physical limits simultaneously. At this juncture, meeting the nano-challenge of IC design exceeds traditional ROI calculations. Although Moore's Law may continue its theoretical path, the cost to FICC to continue on that curve may be prohibitive, as increasing levels of IC and process complexity drive down the hope of profitability.

As we approach 0.10-micron process geometry, CMOS process technology may not continue to provide the same level of cost advantage relative to process development cost. Fewer and fewer companies or government's economic development organizations can afford to make the investments in building state-of-the-art fabs. At these geometries, ownership of intellectual property (IP) and the years of experience behind the IP may favor the well capitalized and experienced and trump the emerging, less experienced.

Also, as often happens when bringing new processes and tooling online it will take longer to reach production yields, and at tremendous costs that will be difficult to amortize (if at all) at exceeding high volumes. So, while we can build the process technology, will it be economically viable? For example, it has been difficult to get production yields at even 0.13-micron process geometries, as the standard assumption for device physics doesn't always act according to plan or require considerable changes in process materials (i.e. copper, low-k dielectrics, deep ultra-violet lithography, etc.). At 90-nanometer real problems occur in materials and lithography.

Design is also experiencing problems as the complexity of the design and smaller geometries conflict with normal movements of electrons at higher frequency and lower power in traditional CMOS processes. To get higher frequencies and lower power, designers are resorting to materials such as silicon germanium (SiGe), silicon on insulator (SOI) and strained silicon. In addition, to pattern these ultra-fine lines designers have had to develop resolution enhancement techniques (RET) or "tricks," such as phase shift mask and optical proximity correction, to produce the patterns necessary.

Because of these factors, FICC must plan up-front for profitability and independent sustainability. New business models will be required to counter the model of creating a fabless firm where the primary goal isn't an IC, but the company's acquisition. In the last few years, many (if not most) fabless semiconductor companies were not created for long-term sustainability, but to be acquired by other larger companies utilizing an acquisition strategy to expand their product and engineering portfolio. Those days are over! Today, a company must be organized and built as an ongoing, sustainable business with real products and product families. Profitability is now a survival issue! The new mantra for fabless semiconductor companies is "real men have profits."

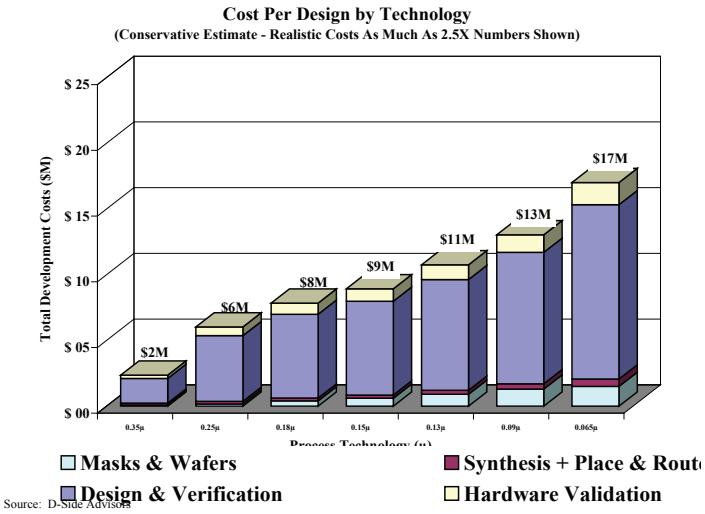
The question today centers on what market and business model

will create profitability. Gone are also the days when financing could be raised by assuming a 10% share of a billion-dollar market. Given the rising costs of design and process, a new firm needs to have a dominant share (say 30% minimum) of a much larger market! Ultimately, fabless semiconductor companies must re-think their business for sustainable profitability in an era when caught between rapidly rising design and process costs and ever-shortening product development cycles.

Design and fab costs higher, customer timelines shorter

Moore's Law propels chip designs to higher levels of integration, and therefore, complexity. The result of increasing chip complexity is more cost added in the form of design expertise and greater amounts of simulation and verification. For example, design costs are rising from $2 million for designs at 0.35-micron to more than $13 million at 0.09-micron.[1] (Figure 1). These costs assume that much of the design and verification can be done in low labor-rate geographies. If not, the costs for a 90-nanometer design could become closer to $30 million. Today, design and verification of complex ICs is now running at 80% of total design cost.

Figure 1



Source: D-Side Advisors

In addition, standard practices need to be closely watched as costs rise. For example, mask and wafer costs are becoming a barrier to many firms with a shallow capital base. With mask costs exceeding $1M at .09µm or 10% of total design costs, design trial and error is too expensive.

Fab costs are also rising to support the relentless march of Moore's Law. IC fab costs are increasing significantly from $1 billion for a 200mm fab at 0.18-micron to more than $3 billion for a 300mm fab at 0.09µm due to:

- Larger wafer size (300mm)
- Copper deposition
- Low-k film dielectrics between copper wires and high-k gate dialectrics for transistor designs
- Esoteric and very expensive lithography methods, which require new photoresists, optical light sources (a mix of 193-nanometer and 248-nanometer deep ultra violet) and resolution enhancement techniques (RET) or optical "tricks" such as phase shift masks and optical proximity correction (OPC).

All of these issues really intensify as production nodes move from 90-nanometer to 65-nanometer. Meanwhile, it seems as if design engineering is caught in 1995 as time to create a design is standing at 18 months to two years. As the customer set shifts to more consumer-based products in the new millennium, this lag time in not acceptable. FICC companies must carefully evaluate risk and return as they are now planning chips at costs exceeding $13 million to be introduced into a market two to three years. To amortize design costs those application markets will need to be a) waiting and b) quite large.

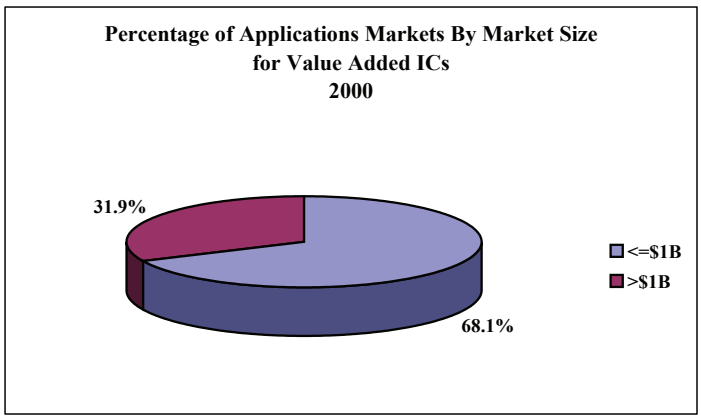
Say Good-Bye to Large Volumes that Amortize Cost

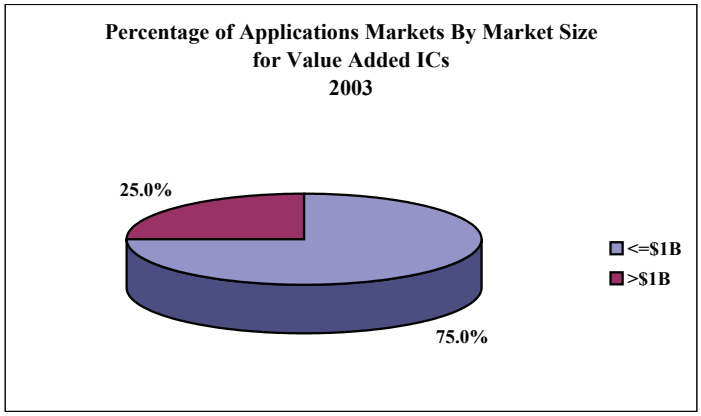
Under the old model, increasing design and process costs simply required higher volume markets to reach profitability. For 25 years expanding markets were there. In the 1990s, these platform application markets included such products as personal computer, cell phones and Ethernet networking.

But today the emphasis is on finer and finer segmentation, and consumer tastes are more fickle and value oriented. Each application-specific integrated circuit (ASIC), application-specific standard product (ASSP) or system-on-chip (SOC) gradually becomes more expensive and requires larger volumes to amortize the cost. This is occurring just as those markets are harder to find. The old financial plan that fab costs will be amortized over a large volume market is gone due to a splintering of product segments and greater pressure to meet customers' time-to-market demands.

For the FICC, it's harder to identify large-volume platform applications. Using data provided by Gartner Dataquest, D-Side Advisors identified 72 application markets that support value added IC designs (i.e. ASICs, ASSPs, field programmable gate arrays (FPGAs), SOCs), which are the primary IC products produced by fabless semiconductor companies. In 2003, of the value-added IC markets identified, 75% of those application markets are $1 billion or less in size of the remaining 25%, and roughly 4% are $2 billion or greater (Figure 2). Just over 50% of the markets are $500 million or less. Remember, that's the total IC market, and there may be several IC vendors targeting that market. So where will the volume come to support all the ASICs, ASSPs, FPGAs and SOCs and amortize the rising design costs brought about by higher integration?

Figure 2.





The end customers may want the functionality and integration of new designs, while simultaneously demanding high reliability and simplicity at fixed product price points ($500, $200, $99, $49). For example, the X-Box, which sells for $199 today, has an IC build cost in excess of $300. At some point there is a limit to losses sustained in the name of market development. How can a vendor reach profitability while shipping dollar bills with each IC sold? Sounds very much like the good old days in the disk drive industry just prior to consolidation. Fabless companies must avoid profitless prosperity and seek markets and business models that will generate sustainable profitability for survival.

Traditionally, IC products derivative from the initial IC development, were where the profits were made. Most likely this will continue to be true if the IC vendor can overcome the initial product cost. On the other hand, if there is no positive return on the initial investment, or if the IC is sold into a narrow niche market, how can a derivative strategy be sustainable?

Example:
Average Cost of New Design (R&D) = $20 million
Cost of Sales (COS) = 50%,
Sales, General and Administrative Costs (SGA) = 25%
Operating Income (OI) = 20%

A $400 million company would need to be created using this example.

FORMULA: Revenue (R) – COS – SGA – R&D = OI solving for R the formula becomes: R – .5R – .25R – 20 = .2R or R = 20/.05 or $400 million.

Assume a minimum revenue requirement using a $20 million design cost (R&D), and also assume a dominant 30% market share would require a $1.3 billion market. What are those markets? According to Gartner/Dataquest, the application markets available to support such cost are less than 15% of all application markets.

Moore's Law Works Against the Success

As Moore's Law breaks the nano barrier the incremental costs of each process step grows exponentially, and the design costs rise to the point where IC profitability is keenly dependent on large platform markets in an era of high segmentation and fickle customers. Moore's Law now will work against the success of a fabless company unless the company clearly understands:

- The market, its growth opportunity, customer requirements and the competitive landscape
- How to creatively reduce costly design architectures
- The need to develop a portfolio of partnerships (customer, design and process) to reduce cost and spread the risk

With the assurance of negative ROI, investment criteria for firms, either foundries or IC vendors, need to be looked at anew. IC design may need to be rethought, not along the lines of how much the industry can continue following Moore's Law, but how to be smart businesspeople. Three suggestions:

- Leverage existing standard IC platforms through software IP
- Shift the emphasis from hardware design to software automation tools and design elements
- Obtain customer commitment earlier through the use of FPGA or micro-controller "breadboards" or proof of concept designs

The fact is that following the current path is a dead end. Increasing levels of complexity lead to higher cost, longer development time and limited profitability and high risk. Yet, given market size and changes in customer needs, new ideas on how to reach profitability are required. ■

References

[1] These costs include mask & wafer costs; synthesis + place & route; design & verification; and hardware validation.

About the Author

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